AMENDMENT TO THE CLAIMS

Please **CANCEL** claim 12.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Original) A method of analyzing timing in an integrated circuit, comprising:

identifying at least one set of racing paths within the integrated circuit, the at least one set of racing paths including an early path and a late path;

identifying at least one delay characteristic of one or more elements in the early path and at least one delay characteristic of one or more elements in the late path;

grouping ones of the one or more elements in the early path with ones of the one or more elements in the late path having similar delay characteristics; and

deriving an adjusted timing slack for the at least one set of racing paths by at least partially canceling delay contributions from grouped elements having similar delay characteristics.

2. (Original) The method of claim 1, wherein the similar delay characteristics comprise correlated delay functions.

3. (Original) The method of claim 2, wherein said deriving comprises:

canceling delay contributions of grouped elements having correlated delay functions;

summing delay contributions of ungrouped elements in the early path;

summing delay contributions of ungrouped elements in the late path;

calculating a delay difference between the early path and the late path by using the summed delay contributions of the ungrouped elements in the early and late paths; and

subtracting the delay difference from an initial timing slack.

4. (Original) The method of claim 3, wherein said summing comprises root sum squaring.

5. (Original) The method of claim 3, wherein the delay difference is a root sum square difference.

6. (Original) The method of claim 3, wherein said deriving further comprises:

calculating metal layer delays for the early and late paths;

summing like metal layer delay contributions in the early and late paths, respectively;

calculating a metal layer delay difference between the metal layer delay contributions for the early path and the metal layer delays for the late path; and

subtracting the metal layer delay difference from an initial timing slack.

7. (Original) The method of claim 6, wherein said summing comprises root sum squaring.

8. (Original) The method of claim 6, wherein the metal layer delay difference is a root sum square difference.

9. (Original) The method of claim 1, wherein the similar delay characteristics comprise location-based delay characteristics.

10. (Original) The method of claim 9, wherein the grouped elements comprise one or more pairs of elements, one element of each of the one or more pairs from the early path and one element of each of the one or more pairs from the late path.

11. (Original) The method of claim 10, wherein said deriving comprises:

computing by using the location-based delay characteristics a variation in a difference in delays of the one or more pairs of elements; and

subtracting the variation in the difference in delays from an initial timing slack.

12. (canceled)

13. (Original) A method of analyzing timing of an integrated circuit, comprising:

tracing at least one set of racing paths;

collecting delay contributions along the set of racing paths;

sorting the delay contributions into groups with similar delay contributions and groups with dissimilar delay contributions;

canceling the delay contributions of the groups with similar delay contributions; and

comparing the delay contributions of the groups with dissimilar delay contributions with an initial timing slack calculated for the set of racing paths.

14. (Original) The method of claim 13, wherein the delay contributions comprise cell-based delay contributions.

15. (Original) The method of claim 13, wherein the delay contributions comprise wire-dependent delay contributions.

16. (Original) The method of claim 13, wherein the delay contributions comprise cell-based and wire-dependent delay contributions.

17. (Original) The method of claim 13, wherein the method further comprises calculating a root sum square delay contribution of the groups with dissimilar delay contributions.

18. (Original) The method of claim 13, wherein the groups with similar delay contributions comprise groups of correlated delay contributions.

19. (Original) The method of claim 13, wherein the integrated circuit is a newly-designed integrated circuit.

20. (Original) The method of claim 13, wherein the integrated circuit is an existing integrated circuit.

21. (Original) The method of claim 13, further comprising:

performing a static timing analysis on the integrated circuit;

identifying a failing test of the static timing analysis; and

using a set of racing paths of the failing test as the at least one set of racing paths.

22. (Original) A computer-readable medium containing instructions that, when executed, cause a computer to perform the method of claim 13.

23. (Original) A method of analyzing timing of an integrated circuit, comprising:

identifying a late path to a timing test and an early path to a timing test;

determining by using location information at least one pair of one element of the late path and one element of the early path;

computing by using the location information a variation in a difference in delays of the elements of the at least one pair; and

deriving from the variation a slack for the late path to the timing test and the early path to the timing test.

24. (Original) The method of claim 23, wherein the at least one pair comprises several pairs.

25. (Original) The method of claim 23, further comprising adding the variation of unpaired elements to the slack.

26. (Original) The method of claim 23, wherein the location information comprises physical location coordinates.

27. (Original) The method of claim 23, further comprising:

performing a static timing analysis on the integrated circuit;

identifying one or more failing tests of the static timing analysis; and

using an early path of the one or more failing tests and a late path of the one or more failing tests as the early path of the timing test and the late path of the timing test, respectively.

28. (Original) The method of claim 23, wherein the integrated circuit is an existing integrated circuit.

29. (Original) The method of claim 23, wherein the integrated circuit is a newly designed integrated circuit.

30. (Previously Presented) A computer-readable medium containing instructions that, when executed, cause a computer to perform the method of claim 23.

31. (Original) A computer-readable medium containing instructions that, when executed, cause a computer to:

identify at least one set of racing paths within the integrated circuit, the at least one set of racing paths including an early path and a late path;

identify at least one delay characteristic of one or more elements in the early path and at least one delay characteristic of one or more elements in the late path;

group ones of the one or more elements in the early path with ones of the one or more elements in the late path having similar delay characteristics; and

derive an adjusted timing slack for the at least one set of racing paths by at least partially canceling delay contributions from grouped elements having similar delay characteristics.

32. (Previously Presented) The method of claim 1, further comprising, prior to the deriving, generating an exposure report containing information on a timing slack for each identified set of racing paths and adjustments that can be made to the timing slack.

33. (Previously Presented) The method of claim 23, further comprising, prior to the deriving, generating an exposure report containing information on a timing slack for each identified path and adjustments that can be made to the timing slack.

34. (Previously Presented) The computer-readable medium of claim 31, further comprising, prior to the derive step, generating an exposure report containing information on a timing slack for each identified set of racing paths and adjustments that can be made to the timing slack.